CLAIMS:

1. A flash-type analog-to-digital (A/D) converter, said A/D converter adapted to convert an input voltage VIN to a digital output, wherein VIN is within a working voltage range of the A/D converter, said working voltage range defined by a lowest voltage VREF- and a highest voltage VREF+, said A/D converter comprising:
N reference voltages V1, V2, ..., VN non-linearly distributed between VREF- and VREF+ and ordered according to VREF- < V1 < V2 < ...< VN < VREF+, wherein N is at least 3;
N comparators associated with said N reference voltages on a one-to-one basis, each comparator adapted to make a comparison between VIN and the reference voltage that is associated with said comparator, each comparator comprising bit-generating means for generating a binary bit that reflects a binary result of said comparison; and
encoder means for generating the digital output from an analysis of the binary bits generated by said bit-generating means.

2. The A/D converter of claim 1, wherein the reference voltages V1, V2, ..., VM-1 are linearly distributed between VREF- and VM, and wherein 1<M<N.

3. The A/D converter of claim 1, wherein the reference voltages V1, V2, ..., VM-1 are linearly distributed between VREF- and VM with a constant reference voltage step size ΔV1, wherein the reference voltages VM+1, ..., VN are linearly distributed between VM and VREF+ with a constant reference voltage step size ΔV2, wherein ΔV1 < ΔV2, and wherein 1<M<N.

4. The A/D converter of claim 1, wherein the reference voltages V1, V2, ..., VM-1 are linearly distributed between VREF- and VM, wherein the reference voltages VM+1, ..., VN are geometrically distributed between VM and VREF+, and wherein 1<M<N.

5. The A/D converter of claim 1, wherein the reference voltages V1, V2, ..., VN are geometrically distributed between VREF- and VREF+.

6. The A/D converter of claim 1, wherein an error in the multibit string relative to VIN (relative error) is a piecewise continuous function of VIN the range of VREF- £VIN

£VREF+, said piecewise continuous function of VIN having a plurality of pieces, wherein each two consecutive pieces of the plurality of pieces are discontinuously joined together, and wherein the relative error within each said piece is a monotonically decreasing function of VIN.

7. The A/D converter of claim 6, wherein each piece of the plurality of pieces has about a same maximum relative error.

8. A method for converting an input voltage VIN to a digital output such that VIN falls between a lowest voltage VREF- to a maximum voltage VREF+, said method comprising:
providing N reference voltages V1, V2, ..., VN non-linearly distributed between VREF- and VREF+ and ordered according to VREF- < V1 < V2 < ...< VN < VREF+, wherein N is at least 3;;
comparing VIN with each of the N reference voltages;
generating a binary bit for each said comparisons, said binary bit reflecting a binary result of said comparison; and
generating the digital output from an analysis of the generated binary bits.

9. The method of claim 8, wherein the reference voltages V1, V2, ..., VM-1 are linearly distributed between VREF- and VM, and wherein 1<M<N.

10. The method of claim 8, wherein the reference voltages V1, V2, ..., VM-1 are linearly distributed between VREF- and VM with a constant reference voltage step size $\Delta V1$, wherein the reference voltages VM+1, ..., VN are linearly distributed between VM and VREF+ with a constant reference voltage step size $\Delta V2$, wherein $\Delta V1 < \Delta V2$, and wherein 1<M<N.

11. The method of claim 8, wherein the reference voltages V1, V2, ..., VM-1 are linearly distributed between VREF- and VM, wherein the reference voltages VM+1, ..., VN are geometrically distributed between VM and VREF+, and wherein 1<M<N.

12. The method of claim 8, wherein the reference voltages V1, V2, ..., VN are geometrically distributed between VREF- and VREF+.

13. The method of claim 8, wherein an error in the multibit string relative to VIN (relative error) is a piecewise continuous function of VIN the range of VREF- £VIN £VREF+, said piecewise continuous function of VIN having a plurality of pieces, wherein each two consecutive pieces of the plurality of pieces are discontinuously joined together, and wherein the relative error within each said piece is a monotonically decreasing function of VIN.

14. The method of claim 13, wherein each piece of the plurality of pieces has about a same maximum relative error.

15. A system for converting an input voltage VIN to a digital output, comprising:
K linear flash-type analog-to-digital (A/D) converter apparatuses Z1, Z2, ..., ZK respectively characterized by reference voltage step sizes $\Delta V1, \Delta V2, ..., \Delta VK$ and respectively adapted to convert VIN into multibit strings S1, S2, ..., SK, wherein $\Delta V1 < \Delta V2 < ... < \Delta VK$, and wherein $K^3 2$; and
encoder means for combining S1, S2, ..., and SK to generate the digital output, wherein the digital output has a sufficient number of bits to preserve the accuracy that is contained within S1, S2, ..., and SK.

16. The system of claim 15, wherein S1, S2, ..., and SK each have a same number of bits.

17. The system of claim 15, wherein S1, S2, ..., and SK do not each have a same number of bits.

18. The system of claim 15, wherein for k=1, 2, ..., K the A/D converter apparatus Zk comprises an arithmetic unit Ak in series with an A/D converter Bk, wherein the A/D converters have a same working voltage range, wherein VIN is within the working voltage range, wherein the working voltage range comprises K contiguous voltage subranges denoted as $\delta V1, \delta V2, ..., \delta VK$ in order of lower to higher voltages, wherein for k=1, 2, ..., K the arithmetic unit Ak is adapted to change VIN into a new input voltage VIN,k in

accordance with a transformation of δVk into the working voltage range and A/D converter Bk is adapted to transform VIN,k into the multibit string Sk.

19. The system of claim 18, wherein $\delta V1$, $\delta V2$, ..., δVK have values such the relative error of the digital output is a piecewise continuous function of VIN within the working voltage range, said piecewise continuous function of VIN having K pieces, wherein each two consecutive pieces of the K pieces are discontinuously joined together, wherein the relative error within each said piece of the K pieces is a monotonically decreasing function of VIN, and wherein each piece of the K pieces has about a same maximum relative error.

20. The system of claim 15, wherein K=2, wherein the A/D converter apparatuses Z1 and Z2 comprise A/D converters B1 and B2 having working voltage ranges $\delta 1$ and $\delta 2$, respectively, such that $\delta 2$ is a subset of $\delta 1$ and $\delta 2/\delta 1$ is an integer subject to $\delta 2/\delta 1 > 1$, wherein B1 and B2 are respectively adapted to convert VIN to S1 and S2, and wherein the encoder means is adapted to generate the digital output as S2 if S2 is not within the voltage range $\delta 1$ else the encoder means is adapted to generate the digital output as S1 multiplied by $\delta 2/\delta 1$.

21. The system of claim 20, wherein $\delta 2/\delta 1 = 2J$, and wherein J is a positive integer.

22. A method for converting an input voltage VIN to a digital output, comprising:
providing K linear flash-type analog-to-digital (A/D) converter apparatuses Z1, Z2, ..., ZK respectively characterized by reference voltage step sizes $\Delta V1$, $\Delta V2$, ..., ΔVK, wherein $\Delta V1 < \Delta V2 < ... < \Delta VK$, and wherein $K^3 2$;
converting VIN, by converter apparatuses Z1, Z2, ..., ZK, into multibit strings S1, S2, ..., SK, respectively; and
combining S1, S2, ..., and SK to generate the digital output, wherein the digital output has a sufficient number of bits to preserve the accuracy that is contained within S1, S2, ..., and SK.

23. The system of claim 22, wherein S1, S2, ..., and SK each have a same number of bits.

24. The method of claim 22, wherein S1, S2, ..., and SK do not each have a same number of bits.

25. The method of claim 22, wherein for k=1, 2, ..., K the A/D converter apparatus Zk comprises an arithmetic unit Ak in series with an A/D converter Bk, wherein the A/D converters have a same working voltage range, wherein VIN is within the working voltage range, wherein the working voltage range comprises K contiguous voltage subranges denoted as $\delta V1, \delta V2, ..., \delta VK$ in order of lower to higher voltages, said method further comprising:
changing VIN by the arithmetic unit Ak for k=1, 2, ..., K, into a new input voltage VIN,k in accordance with a transformation of δVk into the working voltage range; and
transforming VIN,k by the A/D converter Bk, into the multibit string Sk.

26. The method of claim 25, wherein $\delta V1, \delta V2, ..., \delta VK$ have values such the relative error of the digital output is a piecewise continuous function of VIN within the working voltage range, said piecewise continuous function of VIN having K pieces, wherein each two consecutive pieces of the K pieces are discontinuously joined together, wherein the relative error within each said piece of the K pieces is a monotonically decreasing function of VIN, and wherein each piece of the K pieces has about a same maximum relative error.

27. The method of claim 22, wherein K=2, wherein the A/D converter apparatuses Z1 and Z2 comprise A/D converters B1 and B2 having working voltage ranges $\delta 1$ and $\delta 2$, respectively, such that $\delta 2$ is a subset of $\delta 1$ and $\delta 2/\delta 1$ is an integer subject to $\delta 2/\delta 1 > 1$, wherein B1 and B2 are respectively adapted to convert VIN to S1 and S2, and wherein said combining includes generating the digital output as essentially S2 if S2 is not within the voltage range $\delta 1$ else said combining includes generating the digital output essentially as S1 multiplied by $\delta 2/\delta 1$.

28. The method of claim 27, wherein $\delta 2/\delta 1 = 2J$, and wherein J is a positive integer.